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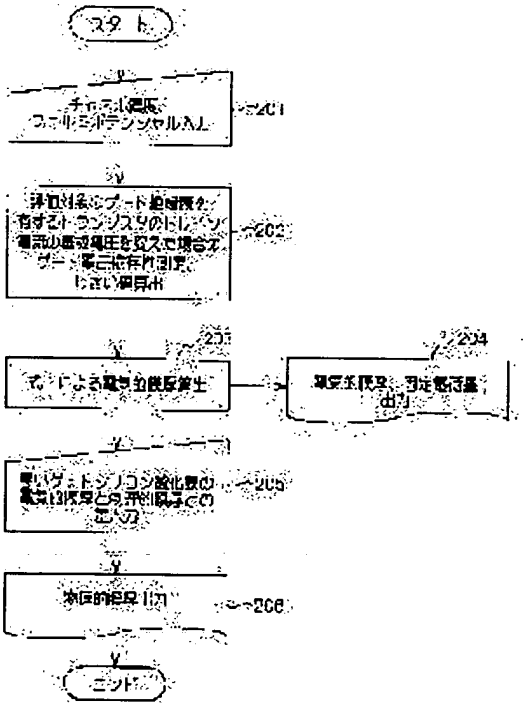
(72)Inventor : TOGO MITSUHIRO

(54) METHOD AND APPARATUS FOR EVALUATING GATE INSULATING FILM

(57)Abstract:

PROBLEM TO BE SOLVED: To accurately evaluate film thickness and film quality of a gate insulating film with respect to the gate insulating film of a field-effect transistor, when the gate leakage current is large or when the film quality or structure is complicated.

SOLUTION: This method of evaluating gate insulating film is to simultaneously form a first field-effect transistor having a first gate insulating film to which C-V measurement is applicable and a second field-effect transistor having a second gate insulating film, to which C-V measurement is not applicable with the same process except for the formation of the gate insulating films, to obtain parameters that are necessary for evaluating the second gate insulating film based on the C-V measurement of the first gate insulating film and the gate voltage dependence of the drain current of the first field-effect transistor by varying the substrate voltage, and to evaluate the second gate insulating film using the parameters.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The first field-effect transistor which has the first gate dielectric film in which C-V measurement is possible, The second field-effect transistor which has the second gate dielectric film in which C-V measurement is impossible Create to coincidence in the same process except formation of gate dielectric film, and it is based on the gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in said C-V measurement and said first field-effect transistor of said first gate dielectric film. The gate-dielectric-film evaluation approach of asking for a parameter required for evaluation of said second gate dielectric film, and evaluating said second gate dielectric film using this parameter.
[Claim 2] The first field-effect transistor which has the first gate dielectric film in which C-V measurement is possible, The second field-effect transistor which has the second gate dielectric film in which C-V measurement is impossible Except formation of gate dielectric film, create to coincidence in the same process and the physical thickness of said first gate dielectric film is measured. The electric thickness of said first gate dielectric film is measured by said C-V measurement. Make the difference of said physical thickness and said electric thickness into parasitic thickness, and the gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in said first field-effect transistor is measured. Based on this gate voltage dependency, the substrate electrical-potential-difference dependency of the threshold electrical potential difference in the first field-effect transistor concerned is computed. It is based on this substrate electrical-potential-difference dependency and the electric thickness of said first gate dielectric film. The first channel concentration concerned and Fermi potential of a field-effect transistor are computed. The gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in said second field-effect transistor is measured. Based on this gate voltage dependency, the substrate electrical-potential-difference dependency of the threshold electrical potential difference in the second field-effect transistor concerned is computed. The gate-dielectric-film evaluation approach which computes the electric thickness of said second gate dielectric film, and computes the physical thickness of the second gate dielectric film concerned based on this substrate electrical-potential-difference dependency, said channel concentration, and Fermi potential from the electric thickness of this second gate dielectric film, and said parasitic thickness.
[Claim 3] The gate-dielectric-film evaluation approach according to claim 1 or 2 which calculates the channel concentration concerned and Fermi potential in self KONSHISU tentorium in case the channel concentration and Fermi potential in said first field-effect transistor are computed.
[Claim 4] The gate-dielectric-film evaluation approach according to claim 2 or 3 which asks for flat band voltage based on the substrate electrical-potential-difference dependency of the

threshold electrical potential difference in said second field-effect transistor, and computes the amount of fixed charges which exists in said second gate dielectric film from the difference of this flat band voltage and ideal flat band voltage.

[Claim 5] The gate-dielectric-film evaluation approach according to claim 2, 3, or 4 which computes interface state density and mobility based on the gate voltage dependency of the drain current in said second field-effect transistor, and the electric thickness of said second gate dielectric film.

[Claim 6] The first field-effect transistor which was created by coincidence in the same process except formation of gate dielectric film and in which physical thickness has the first gate dielectric film in which C-V measurement is possible by known, As opposed to the second field-effect transistor which has the second gate dielectric film in which C-V measurement is impossible The C-V test section which is gate-dielectric-film evaluation equipment for evaluating said gate dielectric film, and carries out C-V measurement of said first gate dielectric film, It has the transistor test section which measures the gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in said first and second field-effect transistor, and operation part. This operation part Based on the C-V measurement result in said C-V test section, the electric thickness of said first gate dielectric film is computed. Make the difference of this electric thickness and said physical thickness into parasitic thickness, and it is based on the gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in said first field-effect transistor measured by said transistor test section. The substrate electrical-potential-difference dependency of the threshold electrical potential difference in the first field-effect transistor concerned is computed. It is based on this substrate electrical-potential-difference dependency and the electric thickness of said first gate dielectric film. The first channel concentration concerned and Fermi potential of a field-effect transistor are computed. It is based on the gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in said second field-effect transistor measured by said transistor test section. The substrate electrical-potential-difference dependency of the threshold electrical potential difference in the second field-effect transistor concerned is computed. Gate-dielectric-film evaluation equipment which computes the electric thickness of said second gate dielectric film, and computes the physical thickness of the second gate dielectric film concerned based on this substrate electrical-potential-difference dependency, said channel concentration, and Fermi potential from the electric thickness of this second gate dielectric film, and said parasitic thickness.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the evaluation approach of gate dielectric film, and evaluation equipment in detail about the evaluation technique of a semiconductor device.
[0002]
[Description of the Prior Art] In the field-effect transistor below 0.15 [mum], since the silicon oxide conversion thickness of gate dielectric film serves as ultra-thin film below 2.5 [nm], a little thickness change is large to a device property, and the design Ruhr influences. Therefore, it is one of the important elements of field-effect transistor development to ask for the thickness and membraneous quality of gate dielectric film correctly in the multipoint on a wafer.
[0003] As the thickness measurement approach of gate dielectric film, cross-section TEM (transmission electron microscope, transmission electron microscope) observation is known. However, by this approach, in order to form the cross-section configuration of a sample, it becomes destructive observation. Moreover, since the creation and observation per sample piece take time amount in case the thickness distribution on a silicon wafer is searched for, it is difficult to observe many samples.
[0004] The approach (C-V measurement: refer to drawing 5) of searching for electrically, using the volumetry of an MOS capacitor as an approach of solving such a problem is learned. Since this technique asks for insulator layer thickness by nondestructive measurement, it has done temporary effectiveness so in searching for the thickness distribution on a silicon wafer.
[0005]
[Problem(s) to be Solved by the Invention] However, in the field-effect transistor to which detailed-ization in recent years progressed, it is becoming difficult to ask for thickness electrically using the volumetry of an MOS capacitor. Because, if the thickness of gate silicon oxide becomes below 2.5 [nm], since a gate leakage current will arise notably, it is because measurement of inversion layer capacity becomes impossible (refer to drawing 6).
[0006]
[Objects of the Invention] Then, since the purpose of this invention has large leakage current, it is to offer the gate-dielectric-film evaluation approach and equipment which can be evaluated also by the gate dielectric film in which C-V measurement is impossible by un-destroying.
[0007]
[Means for Solving the Problem] The first field-effect transistor which has the first gate dielectric film which the gate-dielectric-film evaluation approach concerning this invention can C-V measure, The second field-effect transistor which has the second gate dielectric film in which C-V measurement is impossible Create to coincidence in the same process except formation of gate dielectric film, and it is based on the gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in C-V measurement and the first field-effect transistor of the first gate dielectric film. It asks for a parameter required

for evaluation of the second gate dielectric film, and the second gate dielectric film is evaluated using this parameter.

[0008] Speaking more concretely, the gate-dielectric-film evaluation approach concerning this invention The first field-effect transistor which has the first gate dielectric film in which C-V measurement is possible, The second field-effect transistor which has the second gate dielectric film in which C-V measurement is impossible Except formation of gate dielectric film, create to coincidence in the same process and the physical thickness of the first gate dielectric film is measured. Measure the electric thickness of the first gate dielectric film by C-V measurement, and the difference of the physical thickness of the first gate dielectric film and electric thickness is made into parasitic thickness. The gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in the first field-effect transistor is measured. Based on this gate voltage dependency, the substrate electrical-potential-difference dependency of the threshold electrical potential difference in the first field-effect transistor is computed. It is based on this substrate electrical-potential-difference dependency and the electric thickness of the first gate dielectric film. The first channel concentration and Fermi potential of a field-effect transistor are computed. The gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in the second field-effect transistor is measured. Based on this gate voltage dependency, the substrate electrical-potential-difference dependency of the threshold electrical potential difference in the second field-effect transistor is computed. Based on this substrate electrical-potential-difference dependency, said channel concentration, and Fermi potential, the electric thickness of the second gate dielectric film is computed, and the physical thickness of the second gate dielectric film is computed from the electric thickness of this second gate dielectric film, and said parasitic thickness.

[0009] In case the first channel concentration and Fermi potential in a field-effect transistor are computed at this time, you may make it calculate the channel concentration concerned and Fermi potential in self KONSHISU tentorium.

[0010] Moreover, it asks for flat band voltage based on the substrate electrical-potential-difference dependency of the threshold electrical potential difference in the second field-effect transistor, and you may make it compute the amount of fixed charges which exists in the second gate dielectric film from the difference of this flat band voltage and ideal flat band voltage.

[0011] Furthermore, you may make it compute interface state density and mobility based on the gate voltage dependency of the drain current in the second field-effect transistor, and the electric thickness of the second gate dielectric film.

[0012] The gate-dielectric-film evaluation equipment concerning this invention is what uses the gate-dielectric-film evaluation approach concerning this invention. The first field-effect transistor which was created by coincidence in the same process except formation of gate dielectric film and in which physical thickness has the first gate dielectric film in which C-V measurement is possible by known, As opposed to the second field-effect transistor which has the second gate dielectric film in which C-V measurement is impossible It has the transistor test section which measures the gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in the C-V test section which it is and does C-V measurement of the first gate dielectric film, and the first and the second field-effect transistor for evaluating gate dielectric film, and operation part. And operation part computes the electric thickness of the first gate dielectric film based on the C-V measurement result in a C-V test section. Make the difference of this electric thickness and said physical thickness into parasitic thickness, and it is based on the gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in the first field-effect transistor measured by the transistor test section. The substrate electrical-potential-difference

dependency of the threshold electrical potential difference in the first field-effect transistor is computed. It is based on this substrate electrical-potential-difference dependency and the electric thickness of the first gate dielectric film. The first channel concentration and Fermi potential of a field-effect transistor are computed. It is based on the gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in the second field-effect transistor measured by the transistor test section. The substrate electrical-potential-difference dependency of the threshold electrical potential difference in the second field-effect transistor is computed. Based on this substrate electrical-potential-difference dependency, said channel concentration, and Fermi potential, the electric thickness of the second gate dielectric film is computed, and the physical thickness of the second gate dielectric film is computed from the electric thickness of the second gate dielectric film, and said parasitic thickness.

[0013] Next, about the gate-dielectric-film evaluation approach concerning this invention, language is changed and is explained once again.

[0014] The gate-dielectric-film evaluation approach concerning this invention is characterized by asking for the thickness of gate dielectric film with the substrate electrical-potential-difference dependency of the threshold electrical potential difference in a field-effect transistor. The drain current under the threshold electrical potential difference of a field-effect transistor is large enough compared with a gate leakage current, and a threshold is not influenced of a gate leakage current (refer to drawing 7). Therefore, exact thickness is obtained also in gate dielectric film with a big gate leakage current.

[0015] Moreover, the gate-dielectric-film evaluation approach concerning this invention is characterized by forming the field-effect transistor which has thick silicon oxide as gate dielectric film in the field-effect transistor which has gate dielectric film for evaluation, and coincidence. In the field-effect transistor which has the formed thick silicon oxide as gate dielectric film, in case it asks for the thickness of gate dielectric film by depletion-izing of the impurity in a gate electrode etc., the thickness of electric and physical gate dielectric film can be obtained by removing in quest of the factor used as hindrance, without receiving effect in the structure and membraneous quality in gate dielectric film for evaluation. Furthermore, since thickness can be electrically measured by un-destroying, thickness distribution of the whole silicon wafer surface can be searched for easily.

[0016]

[Embodiment of the Invention] Drawing 1 thru/or drawing 3 are flow charts which show 1 operation gestalt of the gate-dielectric-film evaluation approach concerning this invention. Hereafter, it explains based on these drawings.

[0017] The gate-dielectric-film evaluation approach of this operation gestalt consists of four parts shown in following ** - **.

[0018] ** . The first field-effect transistor which has gate dielectric film which consists of thick silicon oxide, and the second field-effect transistor which has gate dielectric film used as the candidate for evaluation are formed.

[0019] The first and the second field-effect transistor are altogether formed in coincidence using the same process except gate dielectric film. Moreover, the first and the second field-effect transistor may be formed in the same wafer, and may be formed in a separate wafer. In addition, thick silicon oxide is the silicon oxide of the thickness in which C-V measurement is possible, and the gate dielectric film used as the candidate for evaluation is gate dielectric film of the thickness in which C-V measurement is impossible.

[0020] And thick silicon oxide asks for thickness by the ellipsomter or TEM observation. Let this thickness be physical thickness.

[0021] ** . According to the flow chart shown in drawing 1 , the difference of electric thickness and physical thickness and channel concentration are extracted.

[0022] It asks for the thickness of a field-effect transistor which has thick silicon oxide from the inversion layer capacity of C-V measurement (refer to drawing 5). Let this thickness be electric thickness (step 101). ** Search for the difference of the physical thickness for which it set and asked, and the electric thickness for which it asked by C-V measurement as parasitic thickness by the formation of impurity depletion of a gate electrode etc. Let this thickness be parasitic thickness (steps 102-104).
[0023] Then, the gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in the field-effect transistor which has thick silicon oxide is measured (refer to drawing 7). It asks for the threshold electrical potential difference for every substrate electrical potential difference from the relation between the drain current at this time, and gate voltage (refer to drawing 8 , step 105). For example, let the standup electrical potential difference of a drain current when making an axis of abscissa into ******, such as gate voltage, and making an axis of ordinate into ******, such as a drain current, be a threshold electrical potential difference. And the substrate electrical-potential-difference dependency of the threshold electrical potential difference of a field-effect transistor can be expressed with the following formula 1.
[0024]
Vth=(2epsilonSepsilon0qN) (1/2/COX) (VB+2phiF) 1/2+VFB+2phiF ... a formula 1 -- here -- a Vth:threshold electrical potential difference, the specific inductive capacity of epsilonS:silicon, the epsilon0:dielectric constant of vacuum, and q: -- base -- the amount of charges, and N: -- they are channel high impurity concentration, COX:silicon oxidization membrane capacitance, VB:substrate electrical potential difference, phiF:Fermi potential, and VFB:flat band voltage.
[0025] In the relation of the substrate electrical-potential-difference dependency of the threshold electrical potential difference shown in drawing 8 , the variable which inclines (1/2/COX) (2epsilonSepsilon0qN) serves as channel concentration (N) and electric thickness (when the specific inductive capacity of silicon oxide is used for the silicon oxidation membrane capacitance COX in a formula 1, the thickness of gate dielectric film serves as a variable.). The intercept with the y-axis in drawing 8 expresses flat band voltage. Therefore, channel concentration is called for from the electric thickness for which it asked by C-V measurement, and the inclination for which it asked with the substrate electrical-potential-difference dependency of a threshold electrical potential difference. However, since Fermi potential is contained as a function of channel concentration, a formula 1 repeats count until the difference of the channel concentration for which it asked, and the channel concentration set as last time becomes three or less [1017cm -] (steps 106-112). Namely, [0026] which calculates channel concentration and Fermi potential in self KONSHISU tentorium (self-consistent) ** . According to the flow chart shown in drawing 2 , the amount of electric thickness [of the gate dielectric film for evaluation], physical thickness, and fixed charges is extracted.
[0027] In the field-effect transistor which has gate dielectric film for evaluation, the gate voltage dependency of the drain current at the time of changing a substrate electrical potential difference is measured (refer to drawing 7). Next, the graph of the substrate electrical-potential-difference dependency of a threshold electrical potential difference is created (refer to drawing 8). With the inclination in the graph of the substrate electrical-potential-difference dependency of a threshold electrical potential difference, and the channel concentration for which it asked by **, the electric thickness of the gate dielectric film which is a candidate for evaluation is computed (steps 201-203). Moreover, physical thickness is called for by lengthening the parasitic thickness for which it asked by ** from this electric thickness (steps 205-206). Since the specific inductive capacity of silicon oxide is used for the physical thickness for which it asked in the silicon oxidation membrane capacitance COX in a formula 1, it turns into silicon oxide conversion thickness. Moreover, it asks for flat band voltage with an intercept with the y-axis in drawing 8 , and the amount of fixed charges which exists in the gate

dielectric film for evaluation from a difference with ideal flat band voltage is computed (step 204).
[0028] ** . According to the flow chart shown in drawing 3 , the interface state density of the gate dielectric film for evaluation and mobility are computed.
[0029] In the field-effect transistor which has gate dielectric film for evaluation, interface state density and mobility are computed using the gate voltage dependency of a drain current in case there is no substrate electrical potential difference, and the electric thickness of the gate dielectric film for evaluation for which a following formula 2 and following formula 3 list were asked by ** (steps 301-306).
[0030]
S=(kT/q) ln10 (1 (CD+Cit)/COX) ... a formula 2 -- here -- an S:subthreshold level multiplier, k:Boltzmann's constant, T:temperature, and q: -- base -- they are the amount of charges, CD:depletion layer capacitance, the equivalent capacity of Cit:interface state density, and COX:silicon oxidation membrane capacitance.
[0031]
mueff=(dID/dVD) (L/W)/(COX (VG-Vth)) ... a formula 3 -- here -- mueff:effective mobility, ID:drain current, VD:drain electrical potential difference, and L: -- they are gate electrode length, W:gate electrode width of face, COX:silicon oxidation membrane capacitance, the VG:gate electrode, and a Vth:threshold electrical potential difference.
[0032] As the drain current under the threshold electrical potential difference of a field-effect transistor is shown in drawing 7 , compared with a gate leakage current, a threshold is not influenced of a gate leakage current sufficiently greatly (large double or more figures). Therefore, exact thickness can be obtained also in gate dielectric film with a big gate leakage current.
[0033] Moreover, membraneous quality is complicated, and also in the gate dielectric film which specific inductive capacity does not understand, since it can ask for silicon oxide conversion thickness, the gate dielectric film which neither various membraneous qualities nor membrane structure understands can be evaluated. For example, it is suitable for the laminated structure of a silicon acid nitride, a silicon acid nitride, and a high dielectric constant insulator layer etc.
[0034] Drawing 4 is the block diagram showing 1 operation gestalt of the gate-dielectric-film evaluation equipment concerning this invention. Hereafter, it explains based on this drawing.
[0035] The first field-effect transistor from which the gate-dielectric-film evaluation equipment 10 of this operation gestalt was created by coincidence in the same process except formation of gate dielectric film and in which physical thickness has the first gate dielectric film in which C-V measurement is possible by known (not shown), As opposed to the second field-effect transistor (not shown) which has the second gate dielectric film in which C-V measurement is impossible The C-V test section 12 which is for evaluating gate dielectric film and carries out C-V measurement of the first gate dielectric film, It has the transistor test section 14 which measures the gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in the first and the second field-effect transistor, and the microcomputer 16 as operation part. The C-V test section 12 and the transistor test section 14 are constituted by the MOS analyzer 16, the voltage source 18, and the probe needle 20 grade. CRT and printer 22 grade are connected to the microcomputer 16.
[0036] A microcomputer 16 computes the electric thickness of the first gate dielectric film based on the C-V measurement result in the C-V test section 12. Make the difference of this electric thickness and said physical thickness into parasitic thickness, and it is based on the gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in the first field-effect transistor measured by the transistor test section. The substrate electrical-potential-difference dependency of the threshold electrical potential

difference in the first field-effect transistor is computed. It is based on this substrate electrical-potential-difference dependency and the electric thickness of the first gate dielectric film. The first channel concentration and Fermi potential of a field-effect transistor are computed. It is based on the gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in the second field-effect transistor measured by the transistor test section 14. The substrate electrical-potential-difference dependency of the threshold electrical potential difference in the second field-effect transistor is computed. Based on this substrate electrical-potential-difference dependency, said channel concentration, and Fermi potential, the electric thickness of the second gate dielectric film is computed, and the physical thickness of the second gate dielectric film is computed from the electric thickness of the second gate dielectric film, and said parasitic thickness. These functions are realized by the computer program.

[0037] The MOS analyzer 16 measures the current which flows to a field-effect transistor with these electrical potential differences while it changes the output voltage of a voltage source 18 and impressing it to a field-effect transistor as gate voltage, a substrate electrical potential difference, a drain electrical potential difference, etc. Moreover, many field-effect transistors are formed in the wafer 24. A wafer 24 is laid in a prober 26 and moved to X shaft orientations and Y shaft orientations. By having the function in which a microcomputer 16 controls a prober 26, the thickness of the gate dielectric film in a wafer 24 and the field internal division cloth of membraneous quality can be measured automatically.

[0038] In addition, formulas 1 are [the subthreshold level multiplier of a transistor, the relational expression of interface state density, and the formula 3 of the substrate electrical-potential-difference dependency relational expression of the threshold of a transistor and a formula 2] the relational expression of effective mobility and oxide-film thickness. Moreover, it cannot be overemphasized that this invention is not limited to each above-mentioned operation gestalt, but each operation gestalt may be suitably changed within the limits of the technical thought of this invention.

[0039]

[Effect of the Invention] As explained above, when the membraneous quality and structure of the case where the field-effect transistor was made detailed and a gate leakage current becomes large based on the basic configuration of asking for the thickness of gate dielectric film from the substrate electrical-potential-difference dependency of the threshold electrical potential difference in a field-effect transistor, or gate dielectric film become complicated, according to this invention, the thickness and membraneous quality of gate dielectric film can be evaluated correctly, without being influenced of the membraneous quality of gate dielectric film. And since this invention can measure thickness electrically by un-destroying, it can search for thickness distribution of the whole silicon wafer surface.

[0040] If language is changed and is explained once again, the gate-dielectric-film evaluation approach by this invention By forming the field-effect transistor which has thick silicon oxide as gate dielectric film in the field-effect transistor and coincidence which have gate dielectric film for evaluation Using the field-effect transistor in which membraneous quality and thickness have clear thick silicon oxide as gate dielectric film, in case it asks for the thickness of gate dielectric film by depletion-izing of the impurity in a gate electrode etc., stability can be asked for the factor (parasitic thickness) and channel concentration used as hindrance. Consequently, when neither the case where the structure in the gate dielectric film for evaluation is complicated, nor membraneous quality is known, electric and physical gate-dielectric-film thickness can be obtained.

[0041] Therefore, since it can ask for electric thickness when the case where the membraneous quality of gate dielectric film is not known, and a gate leakage current are big gate dielectric film, it can ask for interface state density and mobility (mobility includes the

information on the membraneous quality of gate dielectric film, or the interface of gate dielectric film and a silicon substrate.) from formulas 2 and 3.

[0042] The approach the device property of a field-effect transistor estimates the thickness and membraneous quality of gate dielectric film like this invention is especially effective, when the thickness of gate dielectric film is set to 2.5nm or less by silicon oxide conversion thickness and membraneous quality is known neither by the case where a gate leakage current is big, nor complicated membrane structure. Furthermore, since this invention can measure thickness by un-destroying electrically, it can search for thickness distribution of the whole silicon wafer surface.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the flow chart which shows 1 operation gestalt of the gate-dielectric-film evaluation approach concerning this invention.
[Drawing 2] It is the flow chart which shows 1 operation gestalt of the gate-dielectric-film evaluation approach concerning this invention.
[Drawing 3] It is the flow chart which shows 1 operation gestalt of the gate-dielectric-film evaluation approach concerning this invention.
[Drawing 4] It is the block diagram showing 1 operation gestalt of the gate-dielectric-film evaluation equipment concerning this invention.
[Drawing 5] It is the graph which shows the C-V property of thick silicon oxide.
[Drawing 6] It is the graph which shows the C-V property of thin silicon oxide.
[Drawing 7] It is the graph which shows the gate voltage dependency of the drain current at the time of changing the substrate electrical potential difference in the transistor which has thin gate silicon oxide, and the gate leakage current at that time.
[Drawing 8] It is the graph for which it asked from the data of the graph of drawing 7 and which shows the substrate electrical-potential-difference dependency of a threshold electrical potential difference.
[Description of Notations]
10 Gate-Dielectric-Film Evaluation Equipment
12 C-V Test Section
14 Transistor Test Section
16 Microcomputer (Operation Part)

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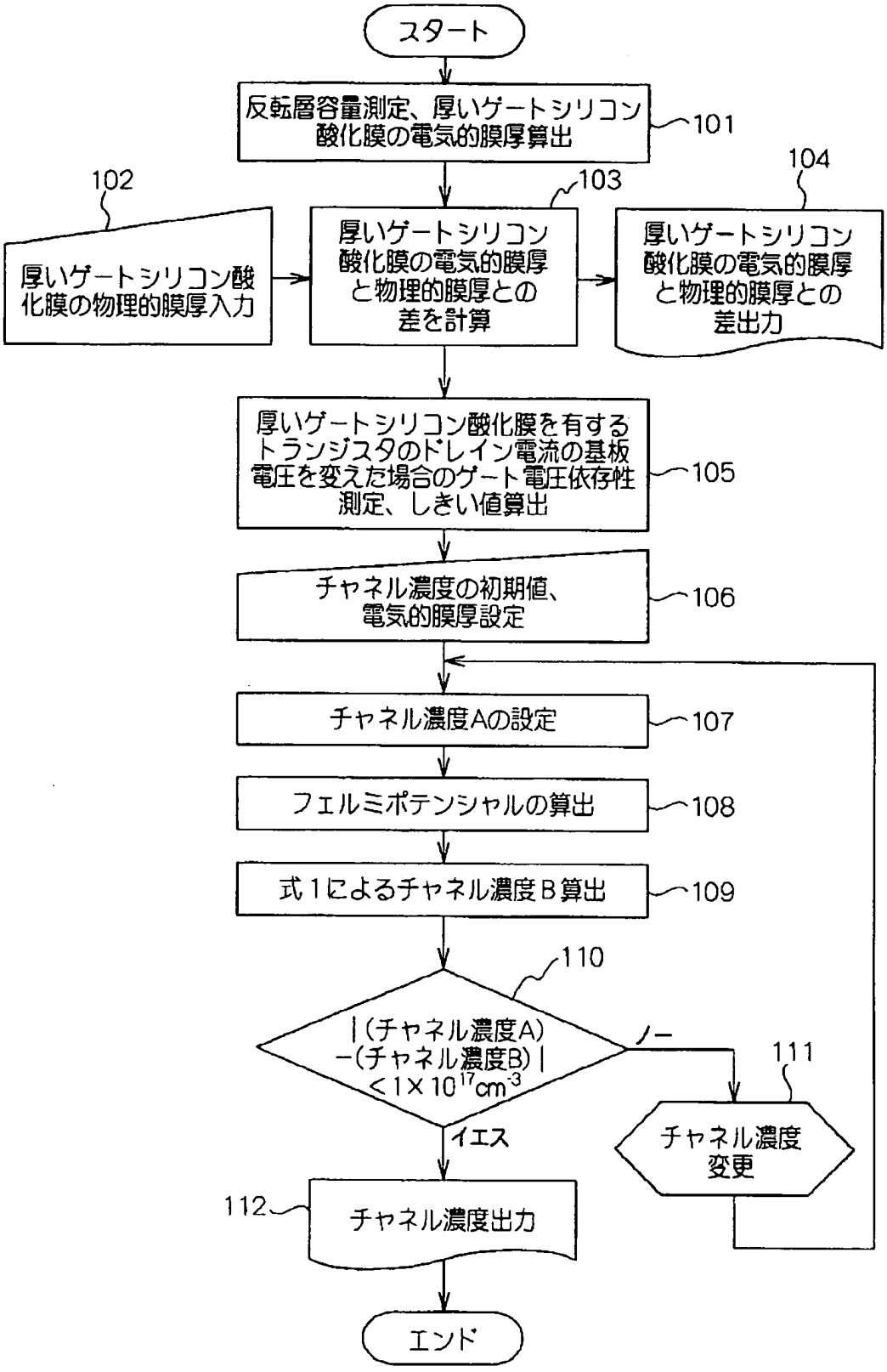
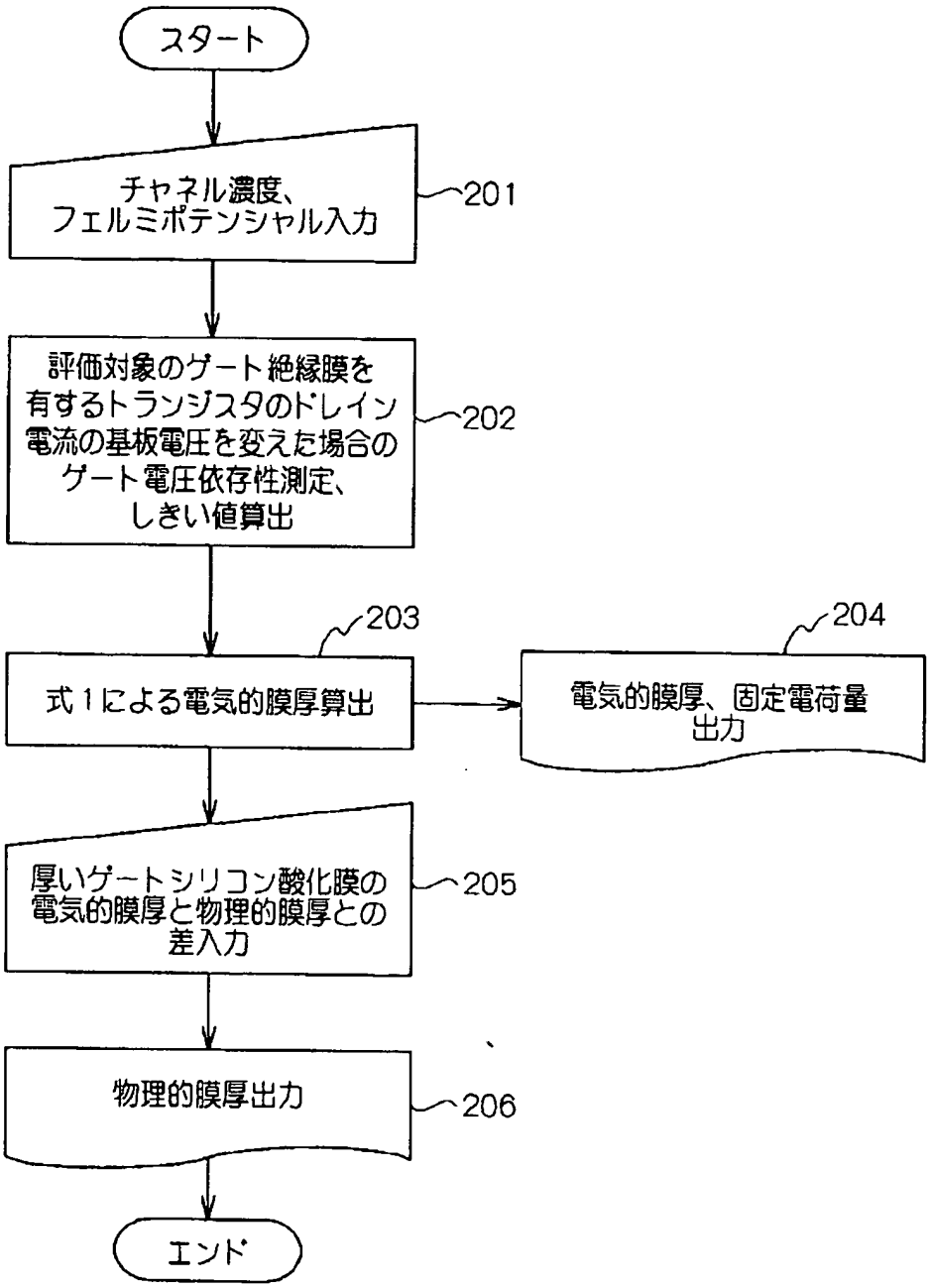
DRAWINGS

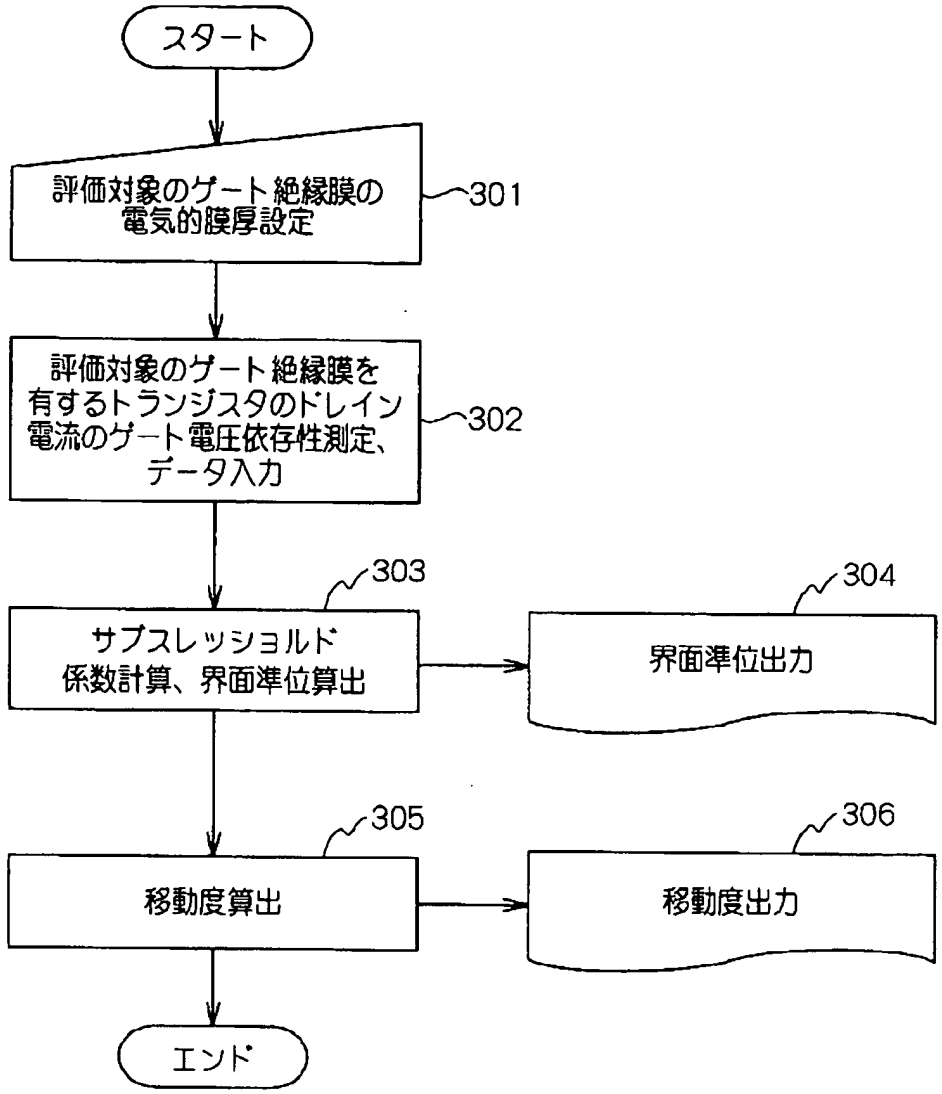
[Drawing 1]


スタート
反転層容量測定、厚いゲートシリコン酸化膜の電気的膜厚算出
101
102
厚いゲートシリコン酸化膜の物理的膜厚入力
103
厚いゲートシリコン酸化膜の電気的膜厚と物理的膜厚との差を計算
104
厚いゲートシリコン酸化膜の電気的膜厚と物理的膜厚との差出力
厚いゲートシリコン酸化膜を有するトランジスタのドレイン電流の基板電圧を変えた場合のゲート電圧依存性測定、しきい値算出
105
チャネル濃度の初期値、電気的膜厚設定
106
チャネル濃度Aの設定
107
フェルミポテンシャルの算出
108
式1によるチャネル濃度B算出
109
110
|(チャネル濃度A)−(チャネル濃度B)|≦1×10^17cm^-3
ノー
111
チャネル濃度変更
イエス
112
チャネル濃度出力
エンド

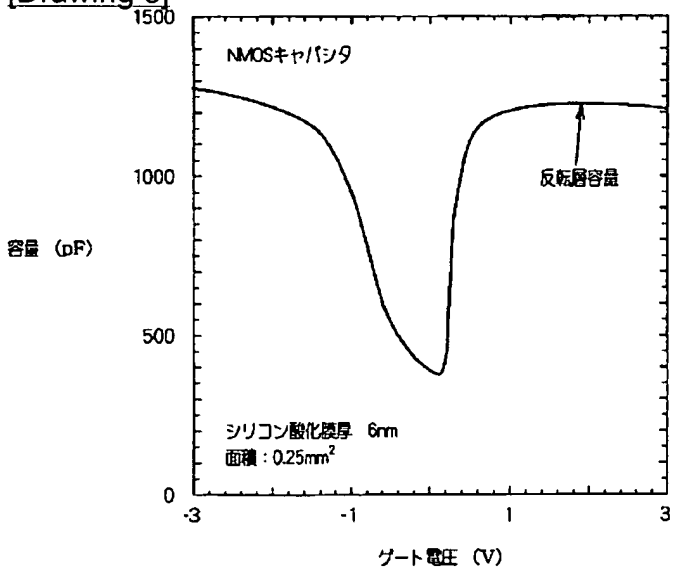
[Drawing 2]


スタート
チャネル濃度、
フェルミポテンシャル入力
201
評価対象のゲート絶縁膜を
有するトランジスタのドレイン
電流の基板電圧を変えた場合の
ゲート電圧依存性測定、
しきい値算出
202
203
式1による電気的膜厚算出
204
電気的膜厚、固定電荷量
出力
厚いゲートシリコン酸化膜の
電気的膜厚と物理的膜厚との
差入力
205
物理的膜厚出力
206
エンド

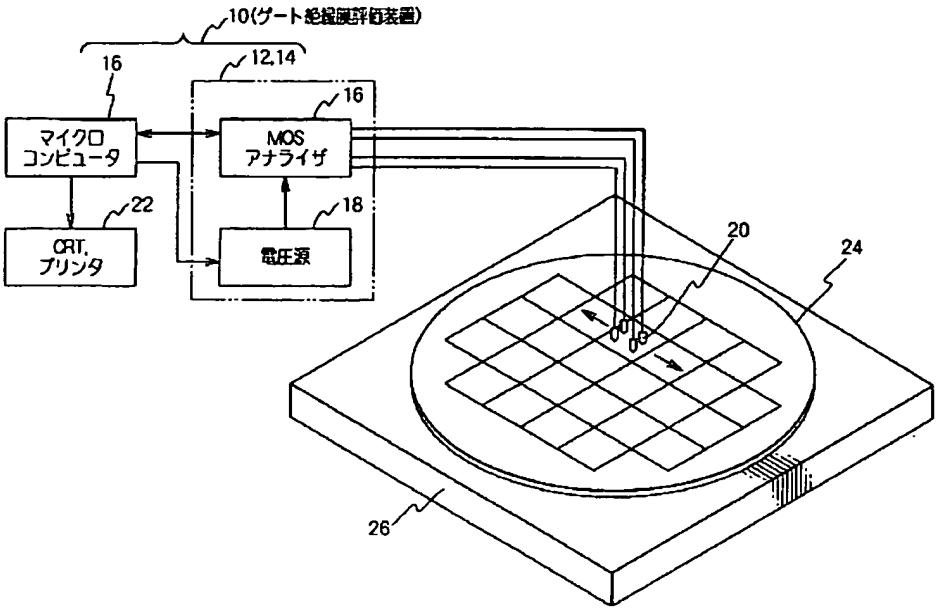
[Drawing 3]



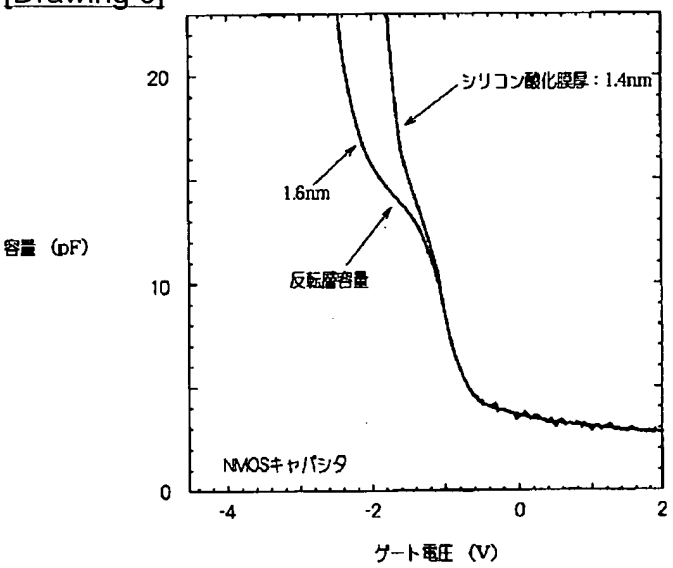
[Drawing 5]



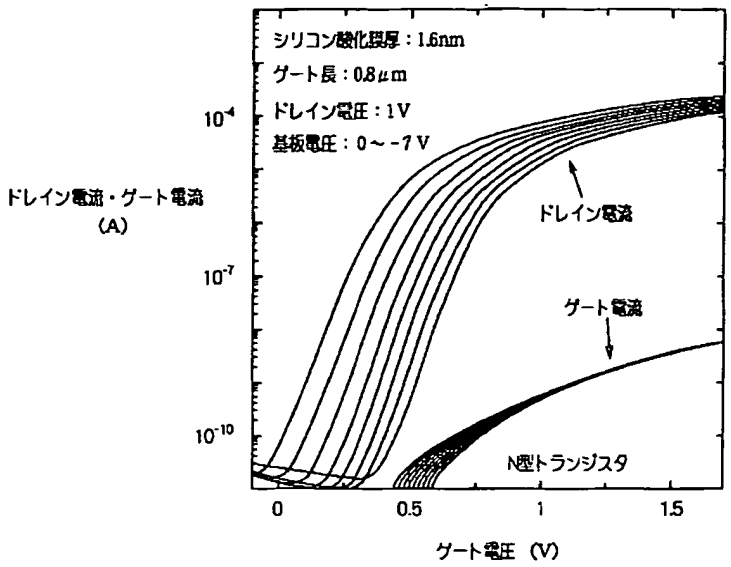
[Drawing 4]



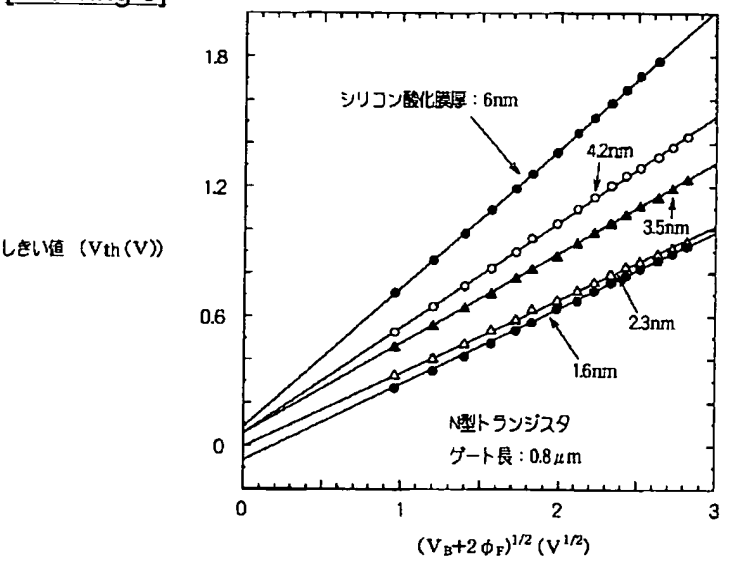
[Drawing 6]



[Drawing 7]



[Drawing 8]



[Translation done.]